In The Claims

Please cancel claims 15-28 without prejudice. Please replace claims 1,3,7,8 and 11-14 with the amended claims 1,3,7,8 and 11-14 as recited below. Please add new claims 29 – 63 as recited below.

1. (Once Amended) A semiconductor device comprising:

a semiconductor substrate having a principal surface of a first conductivity type;

a second conductivity type region, having an island shape, formed on the principal surface of said semiconductor substrate, wherein the second conductivity type region has an impurity concentration profile in a depth direction of the semiconductor substrate;

a first conductivity type region formed inside said second conductivity type region wherein said impurity concentration profile of said second conductivity type region changes gently in the depth direction of the semiconductor substrate and has a gentle peak at a depth that is greater than a junction depth of said first conductivity type region;

a trench formed in the semiconductor substrate extending from a surface of said first conductivity type region to at least said second conductivity type region on said semiconductor substrate;

an insulation film formed on an inner wall surface of said trench; and

an electrode portion made of polycrystalline silicon filling said trench, such that said insulation film is located between said electrode portion and said inner wall surface.

3. (Once Amended) A semiconductor device comprising:

a semiconductor substrate having a principal surface of a first conductivity type;

a second conductivity type region formed on the principal surface of said semiconductor substrate;

a highly doped first conductivity type region formed inside said second conductivity type region;

a plurality of first trenches, each extending from a surface of said highly doped first conductivity type region to reach at least said second conductivity type region on said semiconductor substrate, thereby defining a channel portion on an inner wall surface of each of the first trenches;

an insulation film formed on the inner wall surface of each of the first trenches;

an electrode portion made of polycrystalline silicon filling each of the first trenches such that said insulation film is located between said electrode portion and said inner wall surface;

a plurality of second trenches formed inside said second conductivity type region so that each of the second trenches is positioned between an adjacent pair of said first trenches;

a second conductivity type protrusion region , which protrudes downwardly, wherein the second conductivity type protrusion region forms a junction that is deeper than a junction of said second conductivity type region, the protrusion region being positioned beneath the second trench; and

a second conductivity type highly doped region having an impurity concentration higher than that of the protrusion region, wherein the depth of the second conductivity type highly doped region is less than that of the junction of said protrusion region, the second conductivity type highly doped region is located beneath the second trench, and wherein the protrusion region encompasses the second conductivity type highly doped region.

7. (Once Amended) The semiconductor device according to claim 3, further comprising:

a first electrode provided in one of said second trenches for electrically connecting the second conductivity type protrusion region to the highly doped first conductivity type region through the one of the second trenches;

a second electrode provided in another one of said second trenches for electrically connecting the second conductivity type protrusion region to the highly doped first conductivity type region through the another one of the second trenches, the second electrode being disposed adjacent to the first electrode;

wherein one of adjacent pair of the first and second electrodes is in an electrically floating state.

8. (Once Amended) The semiconductor device according to claim 5, wherein said second conductivity type highly doped region contacts said electrode, and is disposed between the electrode and the second conductivity type protrusion region.

11. (Once Amended) The semiconductor device according to claim 1, further comprising:

a plurality of electric field alleviating regions of the second conductivity type formed in a strip-wise shape so as to enclose a peripheral portion of said second conductivity type region.

12. (Once Amended) The semiconductor device according to claim 11, wherein each of the electric field alleviating regions is composed of:

a strip-wise third trench; and

a second conductivity type deep region encompassing the strip wise third trench.

13. (Once Amended) The semiconductor device according to claim 11, wherein each of the electric field alleviating regions has a pn junction that is deeper than a pn junction of said second conductivity type region.

14. (Once Amended) The semiconductor device according to claim 11, wherein said semiconductor device is constituted as a gate driving type power element for controlling a conduction state between a back surface of said semiconductor substrate and said highly doped first conductivity type region by using said electrode portion as a control electrode.

29. (New) The semiconductor device according to claim 1, wherein the semiconductor substrate comprises:

a second conductivity type semiconductor layer; and

a first conductivity type semiconductor layer located on the second conductivity type semiconductor layer, wherein the principal surface of the first conductivity type is a surface of the semiconductor substrate..

30. (New) The semiconductor device according to claim 3, wherein the semiconductor substrate comprises.

a second conductivity type semiconductor layer; and

a first conductivity type semiconductor layer located on the second conductivity type semiconductor layer, wherein the principal surface of the first conductivity type is a surface of the semiconductor substrate.

31. (New) The semiconductor device according to claim 6, wherein the semiconductor substrate comprises:

a second conductivity type semiconductor layer; and

a first conductivity type semiconductor layer located on the second conductivity type semiconductor layer, wherein the principal surface of the first conductivity type is a surface of the semiconductor substrate.

32. (New) The semiconductor device according to claim 7, wherein the semiconductor substrate comprises:

a second conductivity type semiconductor layer; and

a first conductivity type semiconductor layer located on the second conductivity type semiconductor layer, wherein the principal surface of the first conductivity type is a surface of the semiconductor substrate.

33. (New) The semiconductor device according to claim 12, wherein the semiconductor substrate comprises:

a second conductivity type semiconductor layer; and

a first conductivity type semiconductor layer located on the second conductivity type semiconductor layer, wherein the principal surface of the first conductivity type is a surface of the semiconductor substrate.

34. (New) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type;

a trench MOS structure formed on the first semiconductor layer, wherein the trench MOS structure includes:

a second semiconductor layer of a second conductivity type located on the first semiconductor layer;

a first trench penetrating the second semiconductor layer to the first semiconductor;

a first conductivity type doped region located inside the second semiconductor layer and proximate to an inlet portion of the first trench, thereby a channel portion is defined on a sidewall surface of the first trench between the first conductivity type doped region and the first semiconductor layer;

an insulation film located on an inner wall surface of the first trench;

a gate electrode located in the first trench such that the insulation film is located between the inner wall surface and the gate electrode;

a second trench located in the second conductivity type region and positioned away from the first trench;

a second conductivity type protrusion region having a junction depth that is greater than the junction depth of the second semiconductor layer, the protrusion region being positioned beneath the second trench; and

a second conductivity type doped region that has an impurity concentration higher than that of the protrusion region, wherein the second conductivity type doped region has a diffusion depth that is less than the junction depth of the protrusion region, the second conductivity type doped region is positioned beneath the second trench, and the protrusion region encompasses the second conductivity type doped region; and

an upper electrode, which contacts the first conductivity type doped region of the trench MOS structure through the second trench.

35. (New) The semiconductor device according to claim 34, further comprising a third semiconductor layer of a second conductivity type, the third semiconductor layer being located on a rear surface of the first semiconductor layer, opposite to the second semiconductor layer.

36. (New) The semiconductor device according to claim 35, further comprising a lower electrode contacting the third semiconductor layer.

37. (New) The semiconductor device according to claim 34, wherein the junction depth of the second conductivity type protrusion region is greater than the depth of the first trench.

38. (New) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type;

a trench MOS structure formed on the first semiconductor layer, comprising:

a second semiconductor layer of a second conductivity type located on the first semiconductor layer;

a first trench penetrating the second semiconductor layer to the first semiconductor layer;

a first conductivity type doped region located inside the second semiconductor layer and proximate to an inlet portion of the first trench, wherein a channel portion is defined on a sidewall surface of the first trench between the first conductivity type doped region and the first semiconductor layer;

an insulation film located on an inner wall surface of the first trench; and

a gate electrode located in the first trench such that the insulation film is located between the inner wall surface and the gate electrode;

a second conductivity type island located on the first semiconductor layer and adjacent to the second semiconductor layer of the trench MOS structure, the second conductivity type island being isolated from the second semiconductor layer and being in an electrically floating state; and

an upper electrode, which contacts the first conductivity type doped region of the trench MOS structure through the second trench, wherein the upper electrode is isolated from the second conductivity type island.

39. (New) The semiconductor device according to claim 38, wherein the trench MOS structure further comprises a second conductivity type protrusion region, the junction depth of which is greater than the junction depth of the second semiconductor layer, and wherein the protrusion region is positioned away from the first trench.

40. (New) The semiconductor device according to claim 39, wherein the trench MOS structure further comprises a second trench located in the second conductivity type region and positioned away from the first trench, the protrusion region being positioned beneath the second trench.

41. (New) The semiconductor device according to claim 39, wherein the trench MOS structure further comprises a second conductivity type doped region having an impurity concentration higher than that of the protrusion region, wherein the second conductivity type doped region has a diffusion depth that is less than the junction depth of the protrusion region, and wherein the protrusion region encompasses the second conductivity type doped region.

42. (New) The semiconductor device according to claim 39, wherein the junction depth of the second conductivity type protrusion region is greater than the depth of the first trench.

43. (New) The semiconductor device according to claim 38, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer and opposite to the second conductivity type island.

44. (New) The semiconductor device according to claim 43, further comprising a lower electrode contacting the third semiconductor layer.

45. (New) The semiconductor device according to claim 39, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer and opposite to the second conductivity type island.

46. (New) The semiconductor device according to claim 45, further comprising a lower electrode contacting the third semiconductor layer.

47. (New) The semiconductor device according to claim 41, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer and opposite to the second conductivity type island.

48. (New) The semiconductor device according to claim 47, further comprising a lower electrode contacting the third semiconductor layer.

49. (New) The semiconductor device according to claim 42, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer and opposite to the second conductivity type island.

50. (New) The semiconductor device according to claim 49, further comprising a lower electrode contacting the third semiconductor layer.

51. (New) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type;

a second semiconductor layer of a second conductivity type located on the first semiconductor layer;

a first trench penetrating the second semiconductor layer to the first semiconductor layer, wherein the second semiconductor layer is divided into a first portion and a second portion, the second portion being isolated from the first portion;

a first doped region of a first conductivity type located inside the first portion and proximate to an opening of the first trench;

a second doped region of a first conductivity type located inside the second portion and proximate to the opening of the first trench;

an insulation film located on an inner wall of the first trench;

a gate electrode located in the first trench, wherein a first trench MOS structure is collectively formed with the first semiconductor layer, the first portion and the first doped region, and a second trench MOS structure is collectively formed with the first semiconductor layer, the second portion and the second doped region; and

an upper electrode contacting the first doped region and the first portion of the first trench MOS structure, wherein the second doped region and the second portion of the second trench MOS structure are in an electrically floating state.

52. (New) The semiconductor device according to claim 51, wherein the first trench MOS structure further comprises a second conductivity type protrusion region having a junction depth that is greater than a junction depth of the first portion of the second semiconductor layer, the protrusion region being positioned away from the first trench.

53. (New) The semiconductor device according to claim 52, wherein the first trench MOS structure further comprises a second trench located away from the first trench, the protrusion region being positioned beneath the second trench.

54. (New) The semiconductor device according to claim 52, wherein the first trench MOS structure further comprises a second conductivity type doped region having an impurity concentration higher than that of the protrusion region and having a diffusion depth that is less than the junction depth of the protrusion region, and wherein the protrusion region encompasses the second conductivity type doped region.

55. (New) The semiconductor device according to claim 52, wherein the junction depth of the second conductivity type protrusion region is greater than the depth of the first trench.

56. (New) The semiconductor device according to claim 51, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer.

57. (New) The semiconductor device according to claim 56, further comprising a lower electrode contacting the third semiconductor layer.

58. (New) The semiconductor device according to claim 52, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer.

59. (New) The semiconductor device according to claim 58, further comprising a lower electrode contacting the third semiconductor layer.

60. (New) The semiconductor device according to claim 54, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer.

61. (New) The semiconductor device according to claim 60, further comprising a lower electrode contacting the third semiconductor layer.

62. (New) The semiconductor device according to claim 55, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer.

63. (New) The semiconductor device according to claim 62, further comprising a lower electrode contacting the third semiconductor layer.

CLAIMS SHOWN WITH AMENDMENTS FOR AMENDMENT FILED JULY 29, 2002

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1. (Once Amended) A semiconductor device comprising:

a semiconductor substrate having a principal surface of a first conductivity type;

a second conductivity type region, having an island shape, formed on the principal surface of said semiconductor substrate [by introducing impurities of a second conductivity type by a plurality of ion implantation steps so as to have a smooth] , wherein the second conductivity type region has an impurity concentration profile in a depth direction of the semiconductor substrate;

a first conductivity type region formed inside said second conductivity type region [by introducing impurities of the first conductivity type] wherein said impurity concentration profile of said second conductivity type region changes gently in the depth direction of the semiconductor substrate and has a gentle peak at a depth that is greater than a junction depth of said first conductivity type region;

a trench formed in the semiconductor substrate extending from a surface of said first conductivity type region [so as] to [reach] at least said second conductivity type region on said [first] semiconductor substrate;

an insulation film formed on an inner wall surface of said trench; and

an electrode portion made of polycrystalline silicon [filled in] filling said trench [with said insulation film interposed therebetween] ,such that said insulation film is located between said electrode portion and said inner wall surface.

3. (Once Amended) A semiconductor device comprising:

a semiconductor substrate having a principal surface of a first conductivity type;

a second conductivity type region formed on the principal surface of said semiconductor substrate [having an island shape by introducing impurities of a second conductivity type];

a highly doped first conductivity type region formed inside said second conductivity type region [by introducing impurities of the first conductivity type at high concentration];

a plurality of first trenches, each extending from a surface of said highly doped first conductivity type region [so as] to reach at least said second conductivity type region on said [first] semiconductor substrate, thereby defining a channel portion on an inner wall surface of each of the first trenches;

an insulation film formed on the [an] inner wall surface of each of the first trenches;

an electrode portion made of polycrystalline silicon [filled in] filling each of the first trenches [with said insulation film interposed therebetween] such that said insulation film is located between said electrode portion and said inner wall surface;

a plurality of second trenches formed inside said second conductivity type region so that each of the second trenches is positioned between an adjacent pair of said first trenches [in parallel with said first trenches]; [and]

a second conductivity type protrusion region , which protrudes downwardly, wherein the second conductivity type protrusion region forms [formed with] a junction that is deeper than a junction of said second conductivity type region, the protrusion region being positioned beneath the second trench; and [by introducing impurities of the second conductivity type through each of said second trenches by ion implantation]

a second conductivity type highly doped region having an impurity concentration higher than that of the protrusion region, wherein the depth of the second conductivity type

highly doped region is less than that of the junction of said protrusion region, the second conductivity type highly doped region is located beneath the second trench, and wherein the protrusion region encompasses the second conductivity type highly doped region.

7. (Once Amended) The semiconductor device according to claim 3, further comprising:

a first electrode provided in one of said second trenches for electrically connecting the second conductivity type protrusion region to the highly doped first conductivity type region through the one of the second trenches;

a second electrode provided in another one of said second trenches for electrically connecting the second conductivity type protrusion region to the highly doped first conductivity type region through the another one of the second trenches, the second electrode being disposed adjacent to the first electrode;

wherein one of adjacent pair of the first and second electrodes is in an electrically floating state.

8. (Once Amended) The semiconductor device according to claim 5, wherein said second conductivity type [further comprising a] highly doped region contacts [contacting] said electrode, and is disposed between the electrode and the second conductivity type protrusion region.

11. (Once Amended) The semiconductor device according to claim 1, further comprising:

a plurality of electric field alleviating regions [formed by introducing impurities] of the second conductivity type formed in a strip-wise shape so as to enclose a peripheral portion of said second conductivity type region.

12. (Once Amended) The semiconductor device according to claim 11, wherein each of the electric field alleviating regions is composed of:

a strip-wise third trench; and

a second conductivity type deep region encompassing [formed through] the strip-wise third trench.

13. (Once Amended) The semiconductor device according to claim 11, wherein each of the electric field alleviating regions has a pn junction that is deeper than a pn junction of said second conductivity type region.

14. (Once Amended) The semiconductor device according to claim 11, wherein said semiconductor device is constituted as a gate driving type power element for controlling a conduction state between a back surface of said semiconductor substrate and said highly doped first conductivity type region by using said electrode portion as a control electrode.

29. (New) The semiconductor device according to claim 1, wherein the semiconductor substrate comprises:

a second conductivity type semiconductor layer; and

a first conductivity type semiconductor layer located on the second conductivity type semiconductor layer, wherein the principal surface of the first conductivity type is a surface of the semiconductor substrate..

30. (New) The semiconductor device according to claim 3, wherein the semiconductor substrate comprises:

a second conductivity type semiconductor layer; and

a first conductivity type semiconductor layer located on the second conductivity type semiconductor layer, wherein the principal surface of the first conductivity type is a surface of the semiconductor substrate.

31. (New) The semiconductor device according to claim 6, wherein the semiconductor substrate comprises:

a second conductivity type semiconductor layer; and

a first conductivity type semiconductor layer located on the second conductivity type semiconductor layer, wherein the principal surface of the first conductivity type is a surface of the semiconductor substrate.

32. (New) The semiconductor device according to claim 7, wherein the semiconductor substrate comprises:

a second conductivity type semiconductor layer; and

a first conductivity type semiconductor layer located on the second conductivity type semiconductor layer, wherein the principal surface of the first conductivity type is a surface of the semiconductor substrate.

33. (New) The semiconductor device according to claim 12, wherein the semiconductor substrate comprises:

a second conductivity type semiconductor layer; and

a first conductivity type semiconductor layer located on the second conductivity type semiconductor layer, wherein the principal surface of the first conductivity type is a surface of the semiconductor substrate.

34. (New) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type;

a trench MOS structure formed on the first semiconductor layer, wherein the trench MOS structure includes:

a second semiconductor layer of a second conductivity type located on the first semiconductor layer;

a first trench penetrating the second semiconductor layer to the first semiconductor;

a first conductivity type doped region located inside the second semiconductor layer and proximate to an inlet portion of the first trench, thereby a channel portion is defined on a sidewall surface of the first trench between the first conductivity type doped region and the first semiconductor layer;

an insulation film located on an inner wall surface of the first trench;

a gate electrode located in the first trench such that the insulation film is located between the inner wall surface and the gate electrode;

a second trench located in the second conductivity type region and positioned away from the first trench;

a second conductivity type protrusion region having a junction depth that is greater than the junction depth of the second semiconductor layer, the protrusion region being positioned beneath the second trench; and

a second conductivity type doped region that has an impurity concentration higher than that of the protrusion region, wherein the second conductivity type doped region has a diffusion depth that is less than the junction depth of the protrusion region, the second conductivity type doped region is positioned beneath the second trench, and the protrusion region encompasses the second conductivity type doped region; and

an upper electrode, which contacts the first conductivity type doped region of the trench MOS structure through the second trench.

35. (New) The semiconductor device according to claim 34, further comprising a third semiconductor layer of a second conductivity type, the third semiconductor layer being located on a rear surface of the first semiconductor layer, opposite to the second semiconductor layer.

36. (New) The semiconductor device according to claim 35, further comprising a lower electrode contacting the third semiconductor layer.

37. (New) The semiconductor device according to claim 34, wherein the junction depth of the second conductivity type protrusion region is greater than the depth of the first trench.

38. (New) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type;

a trench MOS structure formed on the first semiconductor layer, comprising:

a second semiconductor layer of a second conductivity type located on the first semiconductor layer;

a first trench penetrating the second semiconductor layer to the first semiconductor layer;

a first conductivity type doped region located inside the second semiconductor layer and proximate to an inlet portion of the first trench, wherein a channel portion is defined on a sidewall surface of the first trench between the first conductivity type doped region and the first semiconductor layer;

an insulation film located on an inner wall surface of the first trench; and

a gate electrode located in the first trench such that the insulation film is located between the inner wall surface and the gate electrode;

a second conductivity type island located on the first semiconductor layer and adjacent to the second semiconductor layer of the trench MOS structure, the second conductivity type island being isolated from the second semiconductor layer and being in an electrically floating state; and

an upper electrode, which contacts the first conductivity type doped region of the trench MOS structure through the second trench, wherein the upper electrode is isolated from the second conductivity type island.

39. (New) The semiconductor device according to claim 38, wherein the trench MOS structure further comprises a second conductivity type protrusion region, the junction depth of which is greater than the junction depth of the second semiconductor layer, and wherein the protrusion region is positioned away from the first trench.

40. (New) The semiconductor device according to claim 39, wherein the trench MOS structure further comprises a second trench located in the second conductivity type region and positioned away from the first trench, the protrusion region being positioned beneath the second trench.

41. (New) The semiconductor device according to claim 39, wherein the trench MOS structure further comprises a second conductivity type doped region having an impurity concentration higher than that of the protrusion region, wherein the second conductivity type doped region has a diffusion depth that is less than the junction depth of the protrusion region, and wherein the protrusion region encompasses the second conductivity type doped region.

42. (New) The semiconductor device according to claim 39, wherein the junction depth of the second conductivity type protrusion region is greater than the depth of the first trench.

43. (New) The semiconductor device according to claim 38, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer and opposite to the second conductivity type island.

44. (New) The semiconductor device according to claim 43, further comprising a lower electrode contacting the third semiconductor layer.

45. (New) The semiconductor device according to claim 39, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer and opposite to the second conductivity type island.

46. (New) The semiconductor device according to claim 45, further comprising a lower electrode contacting the third semiconductor layer.

47. (New) The semiconductor device according to claim 41, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer and opposite to the second conductivity type island.

48. (New) The semiconductor device according to claim 47, further comprising a lower electrode contacting the third semiconductor layer.

49. (New) The semiconductor device according to claim 42, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer and opposite to the second conductivity type island.

50. (New) The semiconductor device according to claim 49, further comprising a lower electrode contacting the third semiconductor layer.

51. (New) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type;

a second semiconductor layer of a second conductivity type located on the first semiconductor layer;

a first trench penetrating the second semiconductor layer to the first semiconductor layer, wherein the second semiconductor layer is divided into a first portion and a second portion, the second portion being isolated from the first portion;

a first doped region of a first conductivity type located inside the first portion and proximate to an opening of the first trench;

a second doped region of a first conductivity type located inside the second portion and proximate to the opening of the first trench;

an insulation film located on an inner wall of the first trench;

a gate electrode located in the first trench, wherein a first trench MOS structure is collectively formed with the first semiconductor layer, the first portion and the first doped region, and a second trench MOS structure is collectively formed with the first semiconductor layer, the second portion and the second doped region; and

an upper electrode contacting the first doped region and the first portion of the first trench MOS structure, wherein the second doped region and the second portion of the second trench MOS structure are in an electrically floating state.

52. (New) The semiconductor device according to claim 51, wherein the first trench MOS structure further comprises a second conductivity type protrusion region having a junction depth that is greater than a junction depth of the first portion of the second semiconductor layer, the protrusion region being positioned away from the first trench.

53. (New) The semiconductor device according to claim 52, wherein the first trench MOS structure further comprises a second trench located away from the first trench, the protrusion region being positioned beneath the second trench.

54. (New) The semiconductor device according to claim 52, wherein the first trench MOS structure further comprises a second conductivity type doped region having an impurity concentration higher than that of the protrusion region and having a diffusion depth that is less than the junction depth of the protrusion region, and wherein the protrusion region encompasses the second conductivity type doped region.

55. (New) The semiconductor device according to claim 52, wherein the junction depth of the second conductivity type protrusion region is greater than the depth of the first trench.

56. (New) The semiconductor device according to claim 51, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer.

57. (New) The semiconductor device according to claim 56, further comprising a lower electrode contacting the third semiconductor layer.

58. (New) The semiconductor device according to claim 52, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer.

59. (New) The semiconductor device according to claim 58, further comprising a lower electrode contacting the third semiconductor layer.

60. (New) The semiconductor device according to claim 54, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer.

61. (New) The semiconductor device according to claim 60, further comprising a lower electrode contacting the third semiconductor layer.

62. (New) The semiconductor device according to claim 55, further comprising a third semiconductor layer of a second conductivity type located on a rear surface of the first semiconductor layer opposite to the second semiconductor layer.

63. (New) The semiconductor device according to claim 62, further comprising a lower electrode contacting the third semiconductor layer.